A FULLY DIFFERENTIAL PHASE-FREQUENCY DETECTOR DESIGN FOR LOW NOISE PHASE LOCKED LOOP APPLICATIONS

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Abstract – *This paper presents a study of phase-frequency detector (PFD) output timing effects on frequency stability of phase locked loops. It is shown that the frequency stability greatly suffers from timing uncertainties. A new fully symmetrical PFD (fd-PFD) design is proposed to overcome the timing issues. It demonstrated significantly improved characteristics over the existing solutions with only minor drawbacks.*

1. INTRODUCTION

Phase-frequency detector (PFD) is one of the key components of frequency synthesizer systems such as Phase-locked loops (PLL) and delay-locked loops (DLL) [1-3]. Since PFD is responsible for comparing phases of the reference and synthesized signals it has critical impact on the loop parameters such as output phase noise and lock time [1]. In this work a special emphasis is made on the effects of PFD timing characteristics on PLL output frequency jitter. Dependence of the phase noise on PFD "up" and "down" signal uncertainties (dead zones) [1, 4] and delays is studied theoretically and confirmed by simulation results. It has been demonstrated that widely used PFD topology [1], alongside with its simplicity and reliability, has a number of drawbacks negatively impacting the loop frequency stability. A fully differential, dead-zone free PFD solution is proposed as an alternative to the conventional architecture.

The introduced modifications demonstrated tangible improvement of PLL jitter, for the price of some increase in layout area.

2. EFFECT OF PFD TIMING ON PLL JITTER

The timing parameters of PFD are often overlooked during low noise PLL design. However for high speed synthesizers PFD up/down signal dead zones as well as the delays may become limiting factors.

Fig.1. shows a schematic diagram of a typical PDF connection to charge pump [1,3] (CP).

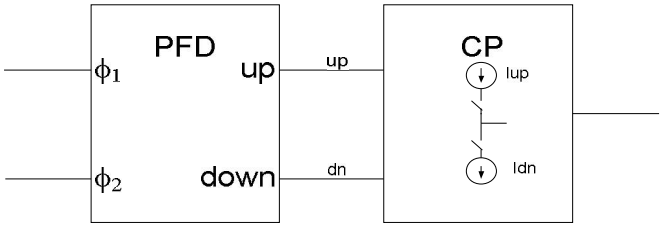

Fig. 1. *Schematic diagram of PFD and charge pump (CP)*

Ideally the PFD compares its input signals, φ_1 and φ_2 in phase and produces "up" and "dn" signals with duration proportional to the input phase difference. The mentioned signals are fed to CP which either sources or sinks current into a low pass filter, creating a control voltage drop across it. When φ_1 and φ_2 signal edges coincide, PFD output should not change. However due to internal timings imperfections the classic three-state PFD [1] produces short false signals (so called dead or blind zones) even when φ_1 and φ_2 are the same in phase. Fig.2 shows an example of such signals with a mutual delay present.

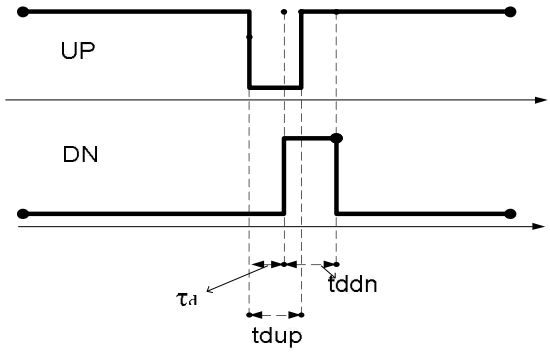

Fig. 2. *Typical PFD timings*

Where tddn and tdup are durations of respectively PFD "dn" (down) and "up" signals and τ_d is the delay between them.

In fact these signals produced in PLL locked state adversely affect its output signal frequency stability. Firstly existence of dead zones implies that PFD sensitivity to input signals edge time differences is limited to τ_{err}=*max { tddn, tdup }*. Hence the loop will be insensitive to phase offset or phase drifts corresponding to τ_{err}. Typical integer PLL frequency dependence on τ_{err} can be presented as follows.

$$f(\tau_{err}) = \frac{f_0}{1 \pm \frac{f_0 * \tau_{err}}{k}}, \qquad (1)$$

Where f_0 is the ideal output frequency of a locked PLL, k is the PLL frequency divider index.

Secondly, PFD spurious signals produced in the locked state cause the charge pump source and sink current into low pass filter, changing its voltage (voltage controlled oscillator-VCO control voltage, vc). As a result these signals induce control voltage ripple which modulates the VCO frequency. Because of this modulation the output frequency constantly fluctuates in time.

The simplest way of characterizing PFD dead zones is expressing them with duty cycle.

$$DC_{up} = \frac{t_{ddn}}{T_{PFD}}, \quad DC_{up} = \frac{t_{ddn}}{T_{PFD}}, \qquad (2)$$

Where DC_{up} and DC_{dn} are correspondingly duty cycles of up and down signals and T_{PFD} is the PFD input signal period.

Assuming the PLL is locked, for PFD inputs the following is correct $\varphi_1 = \varphi_2$. The resulting charge pump current can be presented as:

$$I_{cp} = Ri_{up} * DC_{up} - Ri_{dn} * DC_{dn}, \quad (3)$$

Where Ri_{up} and Ri_{dn} are charge pump current source/sink injection ratios defined as follows:

$$Ri = \int_0^{T_{PFD}} I_{cp}(t)dt, \quad (4)$$

In other words Ri injection ratio is the I_{cp} current supplied by the charge pump during one period of PFD input signal.

As it was mentioned for best ferformance in the locked state $I_{cp} = 0$ condition should take place. From (3) it is seen that this is possible if the following conditions are satisfied:

$$\begin{cases} DC_{up} = DC_{dc} \\ \tau_d = 0 \\ Ri_{up} = Ri_{dn} \end{cases}, \quad (5)$$

Or simply saying, charge pump source and sink currents at any moment compensate each other which is practically hardly achievable especially under varying process, voltage temperature (PVT) conditions.

In equation (3) delay between "up" and "dn" signals was neglected. Taking into account τ_d delay, fig.2 case, the one period charge pump current can be presented by the following expression:

$$I_{cp} = Ri_{up} * DC_{up} - \\ - Ri_{dn} * (2 * \tau'_d + 2 * DC_{dn} - DC_{up}), \quad (6)$$

$$\tau'_d = \frac{\tau_d}{T_{PFD}} \quad (7)$$

The expression (6) shows the charge pump current during one period of PFD operation. Voltage drop (vc) created across low pass filter is proportional to I_{cp}.

Fig.3. shows simulation results for a typical PLL with a 3-state PFD.

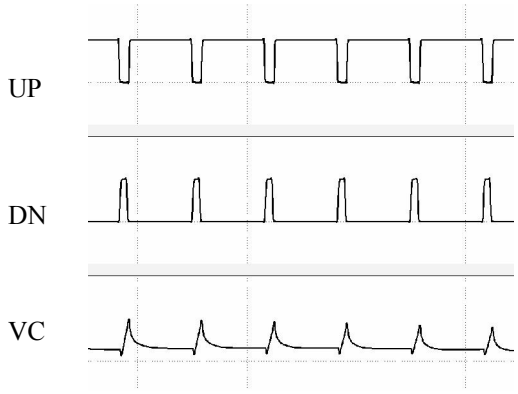

Fig. 3. *Control voltage ripple due to spurious „up" and „down" signals*

UP and DN are the PFD output signals. As it can be seen , although PLL is locked and hence PFD inputs have the same phase and frequency, it still produces narrow UP/DN signals which cause fluctuations of the VC voltage. Jp, period jitter [1] due to control voltage fluctuations can be expressed as follows:

$$Jp = \frac{1}{k_{vco}} \max\left\{\frac{1}{Vc_i} - \frac{1}{Vc_0}\right\}, \quad (8)$$

Where K_{vco} is the VCO gain, Vc_i is the noisy control voltage peak value during i-th period and Vc_0 is the ideal control voltage of a locked PLL. The analytic expression of Vc_i can be derived using (6) and taking into account specifics of the loop filter architecture used in a PLL.

The expression (8) and (6) show that for optimal PLL performance the PFD outputs should produce no signals in a locked state and have minimal mutual delays. To achieve this some modifications to the 3-state PFD are proposed.

3. PROPOSED PFD ARCHITECTURE

A fully differential CMOS PFD for frequency synthesizer applications is presented. This architecture has a number of advantages over the conventional single ended topologies. These advantages include precise timing of output signals (minimal mutual delays, and signal transitions less sensitive to PVT changes), absence of output dead zones false signals as well as improved immunity to voltage source induced noise, and full compatibility with fully differential PLL architectures [1]. The presented architecture is a differential modification of three-state PDF with improved "reset" feedback network, fig.4.

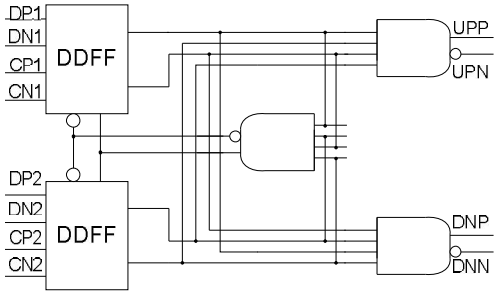

Fig. 4. *Fully differential three state PFD*

The topology consists of differential positive or negative edge triggered D-flip flops and differential AND/NAND elements. The architecture is fully symmetrical as all of its components are differential; this makes its output signal delays equal with great precision. Circuit has eight inputs: DP1, DN1, CP1, CN1, DP2, DN2, CP2, CN2 and four PFD outputs UPP, UPN, DNP and DNN. Signals denoted with "D" are data inputs and their inverse signals, while inputs denoted with "C" stand for DFF clock signals. In normal PFD operation DP1 and DP2 are tied to logic high level voltage while DN1, DN2 are connected to logic low level. CP1 and CN1 come from the PLL reference clock and its inverse; CP2 and CN2 connect to PLL feedback network, i.e. VCO output signals divided by the frequency divider.

For optimal operation the fd-PFD should be used with differential VCO and frequency divider architectures.

The four PFD outputs are connected to the PLL charge pump. Both differential and single-ended charge pump topologies are supported, however the first is preferred as it makes more efficient use of all PFD outputs, insuring optimal timings and noise rejection.

The differential DFF used in the PFD presented here shares common principles with the single-ended, master-slave DFF architectures, fig.5 for a positive edge triggered flop, the master (MS) sub-circuit acquires D input during the negative clock transition. During the positive transition MS enters retention mode while slave (SL) transmits the D value into output. Before being applied to SL signals are buffered with help of a d-AND/NAND element.

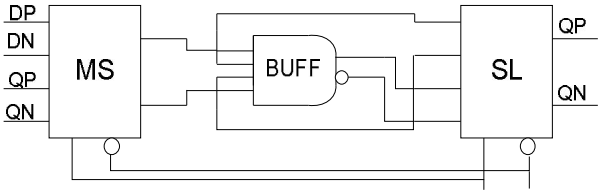

Fig. 5. *Differential DFF architecture*

Unlike the single ended solutions this circuit has two data (DP/DN) and two clock (CP/CN) signals. The outputs QP/QN are correspondingly trigger positive and negative outputs. Fig.6 shows DFF input ("data" and "clock") and output (Q/Qn) signals. Delay between these signals is less than 3pS for the typical PVT corner. For standard single-ended architectures it usually exceeds 30pS due to an inverter present between positive and negative outputs.

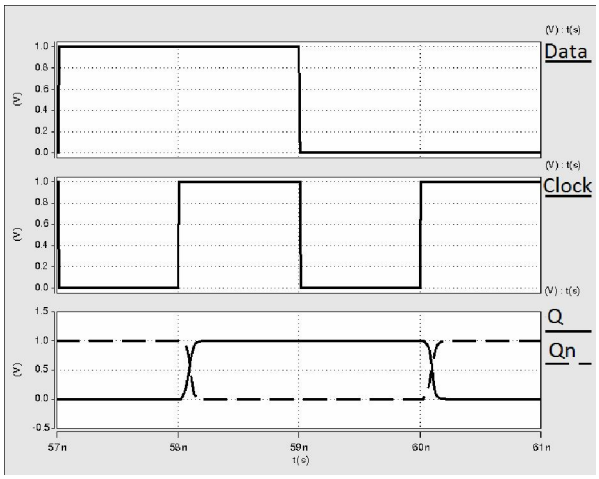

Fig. 6. *Simulation plots demonstrating differential DFF output signals*

The Differential AND/NAND element, widely used in the suggested topology, is a modification of the single ended logic element, fig.7. Output transitions in this circuit are governed mainly by the tail current of MP1 and MN1 transistors. Ideally these tail currents are biased (with VBP and VBN) from a PVT compensated current source, making the circuit timing parameters considerably more stable. The opposite output signals share a negligible delay, which means the circuit simultaneously generates "AND" and "NAND" function of inputs.

The outputs, OUTN and OUTP have shown less than 2ps delay under typical PVT conditions and less than 8ps simulated over 5 PVT corners. This variation can be further decreased by improving the circuit bias current references, i.e. using PVT compensated current references.

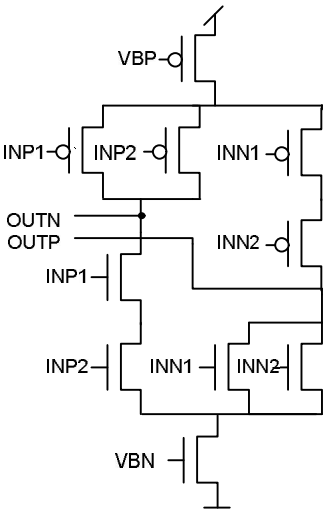

Fig. 7. *Differential AND/NAND cell structure*

Since the output transitions mainly depend on the circuit bias current and load, in contrast with the classic logic gates the circuit exhibits equal output transitions for all input (IN1, IN2, INP1 and INP2) combinations.

The MS/SL blocks of the two stages FF are also designed as fully symmetrical differential architectures, fig.8.

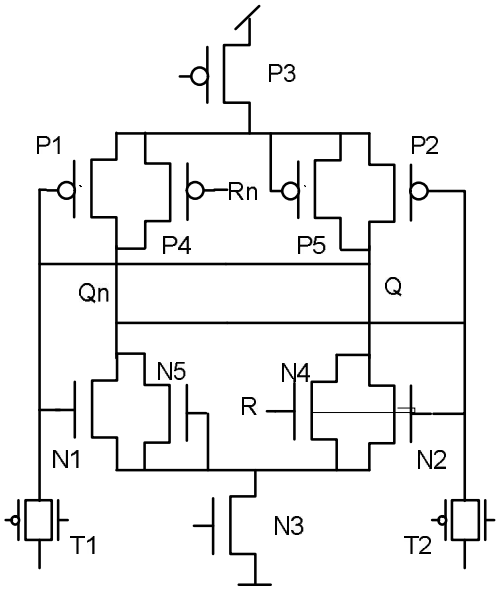

Fig. 8. *Differential MS/SL DFF element*

Here, P1, P2, N1 and N2 devices comprise the main differential amplifier with P3 and N3 tail current sources. P4 and N4 serve as a reset circuitry. With "R" applied high "Qn" is pulled high and "Q" pulled down by respectively P4 and N4. Transistors N5 and P5 are added as dummy replicas of N4 and P4 to preserve full symmetry of the circuit, i.e. to ensure exactly the same capacitive load at Q/Qn outputs. Transmission gates T1 and T2 are the main clocked gates which connect/disconnect the circuit form D/Dn by the clock signal. In the retention mode T1/T2 are disconnected from the loop by inverted clock signals.

For the best performance P3 and N3 are saturated devices acting as current mirrors. Current references resilient to PVT

variations can be used to achieve stable timing characteristics. However depending on the application the mentioned transistors can be connected to logic high or low levels as well.

4. SIMULATION RESULTS AND DISCUSSION

The discussed PFD architecture has been realized in a 45nm CMOS process. Simulations have been performed with the analogue simulator Hspice [5]. The circuit is simulated as separately as within a PLL. A classic, third order [1] 1-2GHz PLL architecture was designed and used for testing purposes. Simulations have been performed over 5 main PVT corners.

Fig.9 portrays negative edge PFD output response for input leading and lagging edges. The first selection of the plot shows the case when the signal "ck" leads the signal "ref". In this case "dn" output produces a positive signal, while the signal "up" is unchanged. It can be seen that no false dead-zone signals are produced. In the selection 2 clock lags reference and a negative up pulse is produced. Again no false switching can be seen at the output "dn".

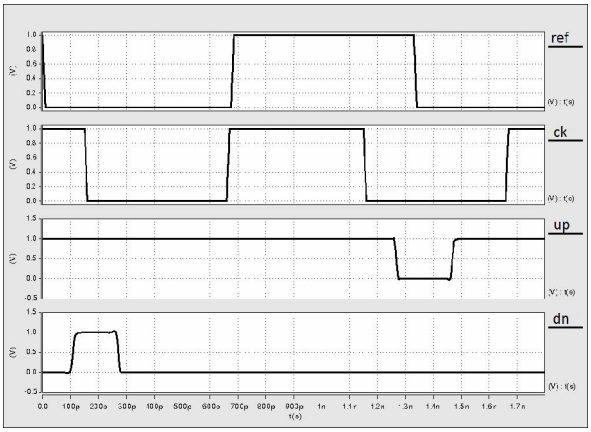

Fig. 9. *PDF output waveforms*

In the case when PLL is locked and PFD input signal edges coincide, in contrary to the waveforms seen in Fig.3 the PFD outputs do not toggle. The latter removes the negative effects of PFD on VCO control voltage improving PLL output signal jitter. Table.1 presents a comparison of the suggested d-PFD and conventional 3-state PFD main parameters in typical PVT conditions.

Table 1. *Simulation results comparing conventional PFD (c-PFD) with fd-PFD*

measurement	fd-PFD	c- PFD	unit
power	3,7	3,9	mW
area	142,8	103,2	uA^2
C2C jitter	45,6	58	pS

Both architectures were tested at 1GHz input frequency. The table shows that the powers in typical corners are close however for the fast PVT corner df-PFD power is 4.2mW vs. 5.9mW of the conventional topology. This is achieved due to stable current biasing of the fd-PFD. C2C jitter is the PLL (locked to 1,5GHz) output cycle-to-cycle (c2c) jitter [1] results obtained with help of simulations. The results show that with the suggested PFD the jitter is decreased by as much as about 21,4 %. Improvement of output signal phase noise is best demonstrated by the signal spectrum. The fig.10 shows the signal spectrum of a PLL with fd-PFD and conventional PFD (marked as c-PFD).

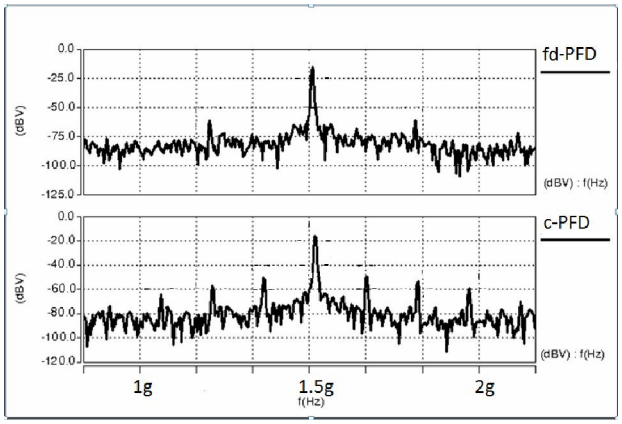

Fig. 10. *PLL signal spectra comparison*

The curve corresponding to the conventional PFD additional frequency-modulation effects, expressed as multiple sideband spurs, can be clearly seen. This modulation is caused by the PFD timing issues described in chapter 2.

The improvement of timing and power parameters is achieved in expense of about 37,3% area overhead, which is a fair trade-off in technologies below 90nm. As meeting jitter specifications for fast developing deep submicron processes and increasing demand for high data rates, becomes more and more difficult. In the meantime area considerations in ultra large scale integration processes cede their positions to reliability and power issues.

5. CONCLUSIONS

The timing uncertainities and excessive delays of PFD output signals have undesired effects on PLL output jitter. A fully differential alternative to the conventional single-ended solution is presented. It has demonstrated tangible improvement of output timings which helped decrease total PLL jitter by over twenty percents for the price of some increase of area.

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