NEW RETENTION FLOP ARCHITECTURE WITH PHASE FREQUENCY DETECTION (PFD) CAPABILITIES

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Abstract – *In this paper conceptually new retention flop architecture for low power applications is presented. The suggested topology has demonstrated timing and efficiency parameters superior to the existing architectures. One of the main advantages of the circuit is the supported high speed operation, and self save and restore capability. Due to its high speed the circuit can also be implemented in phase locked loops within phase detector and frequency divider blocks.*

1. INTRODUCTION

To achieve high density, performance and low cost CMOS technology has been scaled down for several decades. As CMOS technology is scaled power supply and transistor threshold voltages scale down as well in order to maintain the high-speed operation. Although lowering the threshold voltage reduces circuit delays, it also exponentially increases the subthreshold leakage currents. As a result of this leakage power has been continuously growing with every process generation. Now leakage power is responsible for a large portion of total power consumption, reaching as much as 40% to 50% in most technologies.

The power gating technique is the most popular technique to suppress the subthreshold leakage power consumption [1]. The idea of this technique is to cut off a circuit from its power supply rails in standby mode. Due to supply power switched off, the circuit state, which is represented by logic values in sequential elements of the circuit, is lost. Information loses in such systems as processors, memory controllers or peripheral circuitry can have fatal impact on their functionality [2]. For such circuits it is usually necessary to restore the state after returning from power down state. Two main approaches exist for retaining circuit state after power down. The first approach is in using the circuit scan chain, whose original function is testing the circuit state. Mentioned state can be saved on some device, and subsequently restored back into the system after power activation. However this approach is too slow and induces substantial switching power consumption during shifting in/out the circuit state. Usually this approach is used only in applications where sleep period is very long.

The second approach relies on a dedicated circuit element for state retention. Such an element is the flip-flop which is able to retain the state during power gating; it is also called retention flip-flop [3]. In this approach some of the power gated circuit flops are replaced with retention flops. During power down mode the retention flops remember their values and after power activation restore the circuit state.

There are various implementations of retention flops. However in all of these implementations the retention flop operating frequency is lower, than that of a normal flop. All these flops have two externally controlled inputs, by means of which the saving and restoring operation of the flop is carried out. To control these inputs additional logic should be implemented, and the control signals should be connected to it. The physical wiring for these control signals can result in a significant increase of total wire length.

It has been recently reported that the total wire length of power-gated sequential circuits can increase for about 29% to 60% [4]. As a result the dynamic power consumption will drastically increase, and that increase can be even more significant than the total power saved during power gating.

In this work a new type of retention flip-flop is presented which does not have externally controlled save/restore pin. The presented retention flip-flop has very high operating frequency. Moreover the flip-flop has isolation cell capabilities and it can be used as PFD element in Phase locked loops (PLL). Since the flop has very high working frequency, which is one of the important properties of PFD cell.

2. GENERAL PARAMETERS OF RETENTION FLOPS

The retention flop differs from ordinary flop by its data retention and restoration functions. Therefore new parameters should be defined for retention flop to describe these functions. In this section some new parameters of retention flop are presented. These parameters are viable for retention flops and they describe the data retention and restoration capabilities of the retention flop.

The first parameter is data saving time. The data saving time defines the amount of time needed for retention flop to remember the master flop data. Strictly defined, the data saving time is the time that needs to be passed, for the retention logic to remember the master flop data after activation retention command asserted. The equation of data saving time can be written as

$$T_{dsv} = T_{sa} - T_{write}^{ret\_logic} \quad (1)$$

Where T_{dsv} retention is flop data saving time, T_{sa} is the flop saving input activation time and $T_{write}^{ret\_logic}$ is the time when the main flop data is being saved in retention logic.

The data saving time of retention flop can be measured by writing the opposite value of master flop data in the retention logic and measuring the time which is needed to perform the data writing. In case of balloon retention flop saving time is measured by writing some data in balloon latch e.g. logic 0, shifting in the opposite data into master flop e.g. logic 1, then after activating the flop data save input measure the time needed to write the logic 1 value data into balloon register.

Another important parameter is data restoring time. The data restoring time defines the amount of time needed for retention logic to restore the master flop data. Formal definition of retention flop data restoring time is following:

$$T_{drst} = T_{restore}^{mstrflop} - T_{ra}, \quad (2)$$

where T_{drst} is retention flop restoring time, T_{ra} is the flop restore input activation time and $T_{restore}^{mstrflop}$ is the main flop data restoration time. In case of balloon retention flop the flop data restoration time is the time when the flop output value, after power activation, becomes equal to the value saved in retention logic. To measure the worst case restore time initial condition on flop output should be set. So the flop output value should be the opposite value of retention logic saved value. The reason of doing this comes from flop usage. The general flow of restoring retention flop data is following: at first the system power is turned on i.e. power gating of the system is removed, and only after this the flop data restore signal is asserted allowing the retention flop to restore data. When flop power is turned on the flop output gets some X value, this output value is being overwritten by the saved value of retention logic. Hence the flop data restoring time will be the time which is needed for balloon latch to overwrite the Q output value after flop 'restore' input activation. Retention leakage parameter defines the amount of leakage current consumed by the retention part of the retention flop. The measure of this parameter is pretty simple, the retention logic is being simulated separately and the leakage power consumed by that logic is calculated. These three parameters completely describe the functionality of retention logic in retention flop.

3. PROPOSED RETENTION FLOP SCHEME

Generally flip-flop consists of two parts master and slave latches. The function of master latch is to read the flop data and by active clock transfer that data to the slave latch. The slave latch function is to remember the data transferred from master latch. As basic latch structure the cross-coupled inverters are used, this structure is the basic saving element for one bit data [5]. Hence nearly all existing flip-flops use two cross-coupled inverter latches in their architecture. On the other hand the cross-coupled inverters form a feedback system. As a result of the feedback it is not easy to update the data because an input data should "fight" with the feedback. To overcome this effect transmission gate (TG) cell is placed on the cross-coupled inverters path, which switches off the feedback path when data in those inverters should be updated. However, for retention flop this approach is not good, because placed TG increases the retention flop sleep and wake-up times. Therefore in the proposed scheme TG is not placed in cross-coupled inverters path. The next item is master latch, as the main function of master latch is to transfer the input data, hence in the proposed flop scheme the feedback in master latch was removed to increasing flop speed. That latch was replaced by a simple logic which simply transfers the input data. Such solution drastically increases the flop speed. The final scheme of the proposed retention flop is brought in the fig.1.

The flop consists of three parts, next state generation part: I0 inverter and M1 transistor, clocking section M3 to M5 transistors, state retention part M6, M7 transistors and I2, I3 inverters and output isolation part I4 inverter. In functional mode the flop operates in following way: the D input is being inverted by I0 inverter, that inverter is placed for input buffering purposes and the inverted signal is passed to the gate of M1 transistor. By inverted clock signal M2 and M3 transistors are activated and they transfer the input data to M4 and M5 transistors.

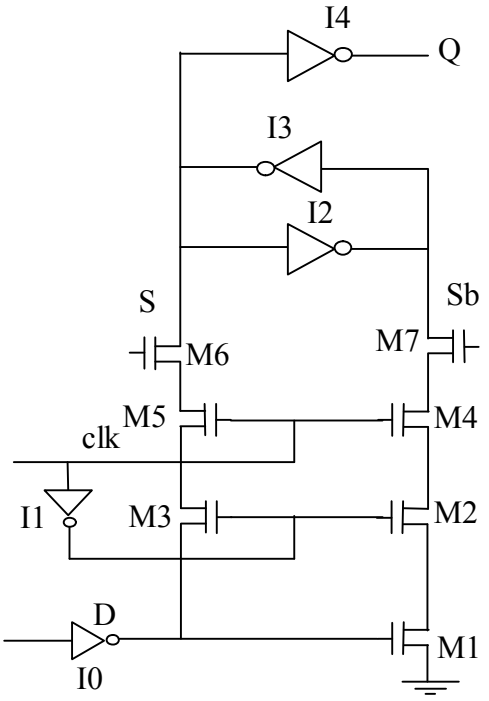

Fig.1. *Proposed retention flop scheme*

These two transistors are placed for isolating the input data from previously read data at the active edge of the clock. During clock positive edge the M4 and M5 transistors are activated and M2, M3 are deactivated. These transistors write the previously read data into the slave latch, consisting of I2 and I3 inverters. It is assumed that M6 and M7 transistors are active in the flop normal functional mode. It can be seen from flop scheme the new data writing in slave I2, I3 latch is being done with two branches S, Sb. These two wires carry the input data and its inverted version; as a result of this the data update speed in slave latch drastically increases. I4 inverter at the output of the flop is placed for output buffering and isolation purposes. In the data retention mode, the M6 and M7 transistors remain inactive hence I2, I3 cross-coupled inverters remember the flop previous state. The I2, I3, I4 inverters are connected to always active power rail. These inverters are implemented with thick oxide transistors; as a result they consume low leakage power when flop is in retention mode. To put the flop into retention mode the clock signal should be kept constant and after that the retention signal can be activated. To restore the flop state only the retention signal must be deactivated. The important property of the flop is that there is no dependence between flop data save and restore signal and clock signal. This decreases the flop power usage as there will be no need for placing additional buffers in 'ret' signal to keep the timing between clock and ret signal. The timing diagram of flop saving and restoring states is shown in fig. 2.

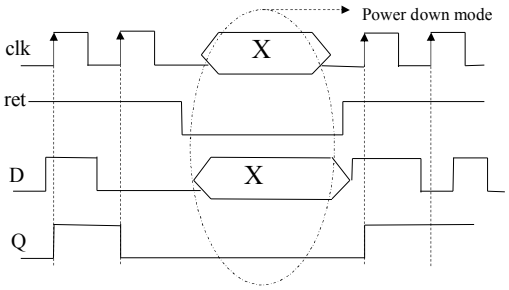

Fig. 2. *Waveform of proposed retention flop*

The flop can serve as isolation cell as well. As it can be seen from flop scheme in power down mode the flop output is equal to retained value. This removes the need for inserting additional isolation cell on flop output for eliminating the sneak paths.

4. SELF RETENTION AND RESTORATION MECHANISM OF THE FLOP

It is known [3] that inserting retention flops in design increases the whole design wiring which significantly increases the total power consumption. In this chapter the question of retention flop control signals wiring will be addressed for the proposed flop. A new mechanism will be discussed which eliminates the need for having retention flop data saving and restoring inputs.

The proposed solution will be discussed in case of footer power gating; however it is acceptable for header power gating as well. In case of footer power gating the footer sleep transistor is placed between the real ground and circuit ground, let's call it virtual ground, [2]. In gating mode that sleep transistor is turned off isolating the real ground from virtual ground. When the footer transistor is turned off the voltage of virtual ground rises towards the supply voltage of the circuit. The virtual ground voltage change can be used for controlling the saving and restoring inputs of the retention flop.

New voltage sensitive circuit is added to flop, which dynamically checks the voltage value of virtual ground. If that value becomes higher than some previously defined save voltage limit, then the sensing circuit writes the flop data into the retention latch and closes the retention M6 and M7 transistors, fig. 1. If the voltage of virtual ground becomes less than the restore voltage limit then the voltage sensitive circuit opens the M6 and M7 transistors and restores the flop state.

Based on above mentioned the proposed retention flop was modified, new schematic part was added to it which can automatically perform the data saving operation. The final flop scheme is shown in the fig. 3.

The voltage sensitive circuit was added to retention flop. This circuit generates 'ret' retention signal in power gating mode. The added circuit contains two PMOS and two NMOS transistors, all these transistors are high threshold transistors in order to reduce leakage power consumption. Since the subthreshold leakage of a MOS device exponentially increases with Vgs, potential difference between Vss and Vdd, a small voltage drop of Vssv from Vdd can cause significant subthreshold leakage from PMOS. To alleviate this stacked inverter is implemented with two PMOS and NMOS transistors.

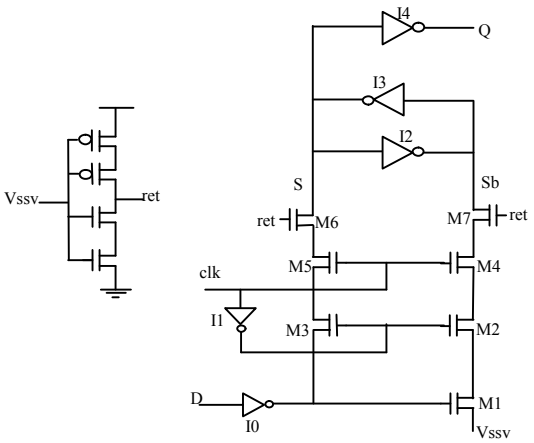

Fig.3. *Self save and restore mechanism of retention flop*

When the footer is power gated the virtual ground voltage Vssv, is starting to rise. That rise after some time causes 'ret' signal value to drop to low level. When the value of 'ret' becomes low, the M6 and M7 transistors are cut-off and retention flop remembers its state. When circuit comes out from the power gating mode then the Vssv input voltage starts to drop and as a result the 'ret' signal goes high , which forces M6 and M7 transistors to open. This can be considered as flop restoring its state and returning to normal functional mode. After this, retention flop starts to operate as a usual flip-flop.

The fig. 4 shows the clk, Vssv, ret signals behavioural in power gating mode.

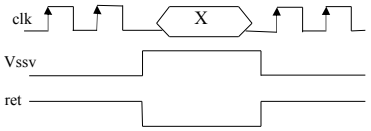

Fig. 4. *Waveform of flop self save and restoring*

5. EXPERIMENTAL RESULTS.

As two new ideas were presented in the article the new retention flop architecture and new structure for performing self save and restore operation, therefore the experimental part of the article consists of two parts. In one part the technical parameters of the suggested flop are analyzed and compared with corresponding parameters of already existing flop parameters.

In the second part the retention flop self save and restore mechanism was analyzed and system level simulations were performed to understand the benefits of proposed solution. As a system level architecture the ChipTop [7] was used. Some cores from Opencores [8] were also used.

The table below shows the comparison of parameters between the proposed flop and the flops presented in [9] reference. All these flops were characterized for the same input and output load. The characterization frequency was 1.5GHz.

Table 1. Comparison of proposed flop parameters with other flops

	Tst	th	tsv	trs	Iret
Proposed flop	10,3p	9,8p	26p	27p	40u
Type I retention flop	15,4p	12,3p	37p	36p	72u
Type II retention flop	16,7	14p	42p	40p	58u
Type III retention flop	12,6	15,3p	43p	44p	64u
Improvement	15%	17%	20%	21%	18%

Where "tst", "th" are the setup and hold times, "tsv", "trs" are the save and restoration times, I_{ret} is the retention leakage and "A" is the flop area.

As it can be seen from the table all parameters of the proposed flop are improved nearly 20%, which is a significant result for 45nm and below technology.

The table below shows the wire length of different benchmarks in comparison with those schemes implemented with proposed flop. All the benchmarks were taken from ISCAS family. By considering s35932 circuit, which is one of ISCAS circuits, it consists of 3300 combinational gates, 1728 flip-flops, and 319 primary outputs.

Table 2: Various benchmarks wire length

	Length (mm)	After proposed flop insertion (mm)
S35932	155.0	147.1
S38417	126.7	116.0
irda1	3.0	2.8
i2c1	5.0	4.2
wb1	46.7	45.1

In experiment the retention saving of benchmark was implemented with two different retention flops. In one case a balloon type retention flop was used, and in second case the proposed flop was used with self save and restore mechanism. The proposed flop and the self saving and restoring mechanism decreases the total wire length because of two reasons. The first is that this flop does not need external wires for controlling the flop save and restore signals. The second reason is that when those wires are removed router is capable to route the remaining wires more effectively. The total wiring also decreases because the isolation cells are removed, as the proposed flop already has isolation cell properties. Hence in the scheme there is no need to place isolation cells, therefore the total wire length and power consumption of the system decreases.

Overall as it can be seen from the table the proposed flop and self saving and restoring mechanism can save the total system power by nearly 18-20%.

6. OTHER APPLICATIONS OF RETENTION FLOPS

Because of its ability to work under high data rates the presented retention flop can be effectively used in frequency synthesizer applications, such as phase locked loops (PLL) and (DLL). The proposed circuit will replace conventional master-slave flip-flop in a three-state phase-frequency detector and frequency divider blocks. Simulations have shown supported frequencies superior to the conventional topologies. Due to the inherent simplicity of the presented retention flop, the PFD based on it has also shown improved immunity to supply noises. Thus for an typical PLL architecture [6] the output period jitter in the presence of supply noise have been reduced by as much as about 6,7%.

CONCLUSIONS

New retention flop scheme was proposed in this work. In the proposed scheme the feedback was removed from master latch to increase the flop operating frequency. The cross-coupled inverters were used as a retention logic, which was tuned for high speed. New mechanism was introduced for retention flop. By means of that mechanism the retention flop can performs its data saving and restoring in power gating mode automatically without any external control signals. This eliminates the need for having two external save and restore inputs for the retention flop, therefore the total wire length of the circuit is decreased. This results in decrease of the power consumed by the circuit wires. Boosting method was proposed for retention flop self save and restore acceleration. This method allows to control the flop sleep and wakeup times. Overall the new architecture presented in this work increases the flop speed nearly 20% and decreases the total circuit power by 15-30%.

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