THE ADVANTAGES OF COMBINING LOW PIN COUNT TEST WITH SCAN COMPRESSION OF VLSI TESTING

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Abstract – *Currently produced digital systems are being of exceptionally high performance and demand testing of VLSI or VVLSI (Very-Very Large Scale Integration) circuit at rates of Gbps. In recent years, we are witnessing significantly fast growth of new techniques for testing of VLSI circuits and systems, which give high quality and fast testing times. Testing at Gbps rates is necessary to overcome traditional techniques, which rely extensively an ATE, and the technology improvements in ICs and their high clock rates [1].*

This requires radical changes in the organization of the test as well as innovative and practical solutions to the support equipment. These changes have a profound impact on many aspects of the existing test techniques.

Low Pin Count Test (LPCT) is a technique which reduces the cost of the test by minimizing the pin requirements of a device when tested on an ATE. When applying LPCT, devices can be easily tested on structural DFT(Design for Testability) testers at high reduced costs, while meeting the low pin count requirements of device and design flow. Combining LPCT with test compression further extends the test capabilities to allow application of all necessary fault models using low-cost testers that are seriously pin-limited. The techniques which are described in this paper represent reduces of test interface and cost of testing and also enable gains in test coverage with less application time and minimal effects on design and test overhead [2].

1. INTRODUCTION

Today's economy and the rising role of new technologies, and expending costs for development of new products, are forcing the electronic industry to reexamine the existing approaches to design and test. For new product, the development of new technological enviroments promises to provide productivity increases and the fastest time to market, while keeping costs under control. Although, testing and debugging of these devices represent very difficult problems; the new economy and modern industry recognizes that the costs of testing are escalating faster than the other costs which are related to the development phase.

1.1 Testing at Gbps rates

For example, allowing high transfer rates among channels and functional units, such as in the I/O definition of a SoC, requires readressing the implication of data format and communication within a serial mode. This contains feature into a shell, that physical phenomenon, such as the jitter, which becomes very relevant to tester operation. It is today's focus on all of these issues which make multigigahertz testing a challenging problem in today's test technology.

The manufacturing test process for ICs is increasing in cost and effort in order to keep up with rigorous quality standards, complexity of newer designs and process nodes, narrower time-to-market windows, and demand to reduce the test pins. High density, core-based ICs have significant popularity, although the complexity of these chips can slowdown the development and the increase cost, rather than enable high performance and profit margins in manufacturing.

DFT engineers are using the advanced fault models to improve the test quality. However, the increasing of test time and volume, which translates into increased cost, is forcing many companies to apply the necessary tests in fewer test cycles and with fewer pins, if possible.

Low Pin Count Test (LPCT) is a technique which reduces the cost of the test by minimizing the pin requirements of a device under test, when tested on an ATE. When applying LPCT, devices can be easily tested on structural DFT testers at dramatically reduced costs while meeting the low pin count requirements of the device and the design flow.

Combining of LPCT with the test compression further extends the test capabilities to allow application of all necessary fault models using low-cost testers that are seriously pin-limited. The LPCT techniques enable gains in test coverage with less application time and minimal effects on design and test overhead.

1.2 Automated test equipment, ATE Interface

The economics of the test, especially in a case of need test equipment in particular, has received a significant attention from many vendors and ATE manufacturers, customers of ATE and the research community at large. The general block scheme of ATE is shown in Fig. 1 [3-4-5].

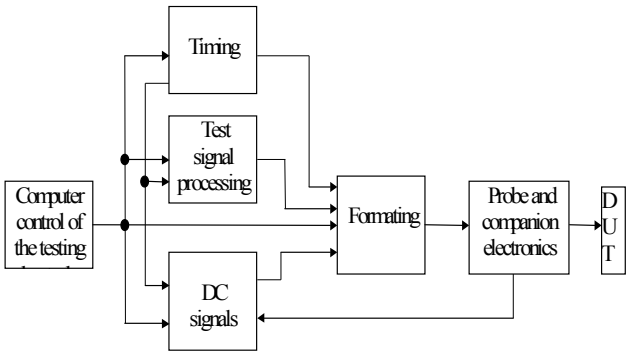

Fig.1. *Architecture of a electronic tester, ATE*

The increasing cost of the ATE increases the price of the product. The features, such as multisite organization, architecture modularization, and the increased presence of inexpensive testers such as those included in BIST techniques (BIST - Built In Self Test), are some of the significant developments in recent years. As one possible alternative for speeding up the test application time occurs a combination of BIST and ATE [4].

The rigorous quality standards for manufacturing test of ICs, the complexity of newer technology nodes, and narrower time-to-market windows are increasing the cost and the effort to test the manufactured parts.

To improve the test quality, the DFT engineers are using advanced fault models, such as transition, path-delay, multiple-detect, bridging, etc., which intention is the catching of the additional defects, which are missed by the conventional stuck-at fault model.

There are two areas contributing to the increasing costs: the growing test data volume and the cost of the automatic test equipment (ATE). Each of these advanced fault models requires complex test sets, which are much bigger in size when compared to a conventional stuck-at pattern test set. The growing circuit size and support for other fault models increases the test data volume that has to be stored inside a tester and the test application time, which is directly proportional to the volume of test data shifted into the circuit via scan chains.

In order to extend life of the existing testers which are limited in the number of pins they support, a smaller tester interface is needed. This is achieved through reduction of dedicated pins required for test as well as functional pins that must be controlled and observed during test application. Specific test pins include tester scan channels, test control signals such as scan enable, and test clocks. Reducing the test and functional I/O pin interface to the tester, enables the use of cheaper testers that do not support large number of pins. This approach also simplifies design and manufacture of tester heads which can be very costly.

2. THE ECONOMICS OF TEST

The cost of an ATE is non-linearly proportional to the number of pins it can support, operating frequency, pin electronics, and memory per pin. As the operating frequency of the devices increases, packages become more complex, the demand for scan memory keeps on rising, and the infrastructure cost to support test increases exponentially, affecting the profit of a product.

A purchase price of one tester can be calculated by using the following formula

$$C = b + \sum (m \cdot x) \qquad (1)$$

where C represents the cost, and the representations of the other values can be viewed in Table I. This also requires adding of costs of a tester's life cycle, such as amortization and obsolescence, maintenance, costs of work (energy, replacable components and similar) [5].

Today, many producers of testing devices exist. Depending on configuration one tester of high performance may cost a couple of millions dollar and more [6]. High quality probe and catcher, cost up to half milion dollar.

This has forced many companies to move from the full-bandwidth, at-speed functional testing to low-pin-interface structural test. In such cases, the ATE is able to perform structural testing effectively by using a scan for control and observability and internal PLLs for high-frequency clocking, but cannot perform functional testing. To overcome this limitation, sufficient testing must be incorporated into the device to ensure high fault coverage for structural testing and to ensure test quality, so that functional tests can be reduced drastically.

One of the common considerations for the Low Pin Count Test (LPCT) is a top-level chip routing, which can cause congestion in modular designs. The applying of the high quality test to each block, using as few as 1 or 2 channels, significantly reduces routing congestion. Other common test techniques for wafer and multi-site testing also benefit greatly from LPCT. Tester and design pin limitations can also limit the number of available pins for the test, thus mandating a low pin count test approach.

TABLE I. THE PRICES OF TESTERS

Possibilities of testers	Basic price (b)	Price by pin (m)	Number of pins (x)
	k$	$	
ASIC and µprocessor of high performances	250 – 400	2.700 – 6.000	512
Systems with mixed signals	250 – 350	3.000 – 18.000	128 – 192
DfT Tester	100 – 350	150 – 650	512 – 2500
ASIC and µcontroller of low performances	200 – 350	1.200 – 2.500	256 – 1.024
Memory chips	200+	800 – 1.000	1.024
RF	200+	~50.000	32

3. LOW PIN COUNT TEST SOLUTIONS

The following section describes and summarizes several LPCT methodologies that have been implemented to meet various designs and test requirements.

Even in some extreme LPCT applications, such as the 3-pin Tessent™ TestKompress® methodology described in this paper, high data and test time compression ratios greater than 25x have been demonstrated with no impact on the test coverage. When functional pin access is provided by using boundary scan cells, higher test coverage of logic between the scan cells and the top-level pins can be achieved.

The focus is on manufacturing test which requires high quality deterministic test patterns which can effectively identify manufacturing defects in silicon. Low Pin Count Testing provides an effective manufacturing test methodology, which means that those devices can be tested with high quality deterministic test patterns and in a cost effective manner. This is achieved by reducing the number of pins which come in contact with the tester during execution of structural test for the device. Various design and test requirements drive the need to reduce the number of pins in the tester interface. This includes scan and test control pins

and functional pins, in some cases. Many of the common motivations for LPCT are listed below.

3.1. Design Pin Limitations

Corresponding electronics, that is a board for interface with device or circuit under test (DUT-CUT), DIB (Device Interface Board), represents electrical interface between ATE and DUT. There are various form and size of DIB, but their common functions are to provide reliable and uncomplicated separable electrical interface between DUT and electrical instruments of the tester.

VLSI testers, that are available on the market, may satisfy different needs. In contrast to PCs, testers have no standard architecture. Every producer of testing equipment is trying to apply some unique performance in order to complete with rival producers. Different producers of testing equipment build their own S/W platform for testing. Moreover, test routines developed for one type of tester frequently are very difficulty to translate for use on other testers because of H/W optimization to testers. Fortunately, the majority of automatic tester has many common functions and features.

Beyond the chip-level test interface, LPCT provides a significant value in reducing the chip top level routing and congestion. Today's modular design practices require a reduction to the number of connections between cores and top level pins. LPCT enables application of test data with very few pins while maintaining the ability to apply a high quality deterministic patterns to each core with minimal test interface routed to each I/O pin.

Although designs continue to grow in size, package pins have not maintained the same growth rate. In fact, many applications require fewer pins despite the gate count increase. In addition, an increase in the number of required analogue pins is reducing the number of digital pins available for digital test. Similarly, mixed-signal designs with small digital content may have as few as three digital pins, thus greatly complicating scan test.

3.2 Wafer Test application

One of the challenges of wafer test application is the number of contacts that the test head must make with each die on the wafer. Each additional contact point results in additional cost due to the required precision and accuracy and the risk of poor contact. There's also potential for damage to the die as a result of each contact. By minimizing the test and functional interface requirements, LPCT addresses these concerns and ensures that yield is not reduced as a result of wafer test. Designs with multiple test access interfaces can be configured with fewer pins for wafer test while still providing a full pin interface for package test.

To avoid the one hours work of analyzing all failures, we developed a metodology to correlate electrical failures to particular process steps[7]. In this step, we used metodology that dedicated inline defectivity inspections during fabrication. Comparing the wafer imagines with the layout, we can use a third-party tool to identify abnormalities.

3.3 Multi-site Testing

A smaller test interface is required for effective application of the same test patterns to multiple devices in parallel. This technique, called multi-site testing, multiplies the value of scan compression by simultaneous test data application and observation. Low pin count test increases the number of devices that can be tested in parallel, greatly reducing test application time and test cost. Although not limited to wafer test, multi-site testing is most commonly used during wafer test.

3.3 High Quality Test at Board and System Levels

A common test methodology for board and system level test is Built-in Self-Test (BIST), shown on Fig.2., which applies pseudorandom patterns to the device and compresses the circuit responses into a signature [6].

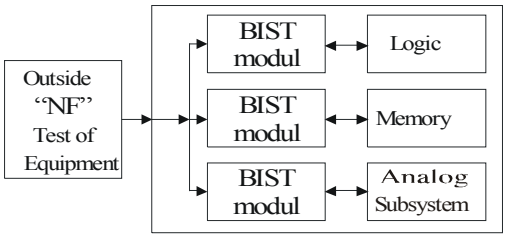

Fig.2. *Architecture of chip with built in self-test.*

However, some devices may not be suitable for BIST and require in-system test patterns that target specific defect mechanisms deterministically. In order to apply deterministic patterns in system, a low pin count interface such as the standard IEEE 1149.x Test Access Port (TAP) is required. The 4 or 5 pin TAP interface standardized chip-level access across the board and is commonly used to apply tests at board and system test.

3.4 Low Channel Tessent TestKompress

For many designs, Tessent TestKompress alone can meet the reduced pin count requirements by reducing the scan interface to the tester.

The Tessent TestKompress decompressor (Fig. 3.) is uniquely capable of encoding significant data through very few scan channels, enabling it to achieve high compression of test data and test application time with very few scan channels. Using patented technology, the compactor expands this capability further in the presence of unknown (X) states.

In order to reduce pin count in cores or chip level of designs, Tessent TestKompress can apply high quality deterministic test patterns with as few as 1 scan channel. This can greatly simplify top level routing for cores and simplify the tester interface for chip level, wafer, and package tests. Aggressive compression by using only 1 or 2 channels can be achieved with the dramatic results.

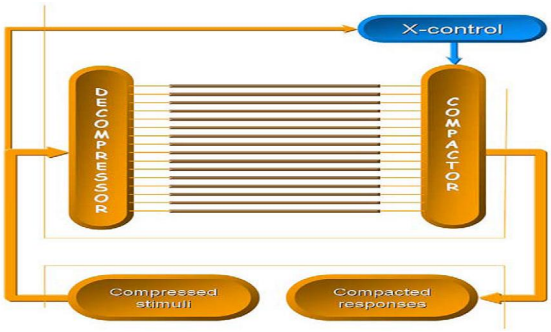

Fig.3. *Tessent TestKompress Architecture*

For modular designs with several implementations of low channel Tessent TestKompress logic, a significant reduction in top level routing and block interface can be achieved. Additionally, identical blocks can share inputs that broadcast the test stimuli and further reduce test pins.

Another key requirement for manufacturing test is effective and accurate diagnosis. Tessent TestKompress patterns can be diagnosed during manufacturing with the same accuracy of uncompressed patterns using Tessent Diagnosis. This enables online diagnosis of failing devices on the manufacturing floor without the need for offline application of bypass patterns.

3.5 Functional Pin Access through TAP

A standard scan methodology requires the tester to connect to all device pins in order to apply scan data through the scan I/O, drive values on the functional primary input pins and to observe circuit responses on the functional primary output pins. The basis of ideas that allows the implementation of these requirements is to add cell shift register with each input/output interface components.

The structure of the system that was designed to BS concept, it should contain at least four additional connections per PCB or chip, which is related to the signals TDI(Test Data In), TDO(Test data Out), TMS(Test Mode Select) and TCK(Test clock). The topological and functional, these signals must be processed before they lead to very "cells." This set of connections is required and is known as Test Access Port or TAP for short. Of course, as we have seen, the topological and functional, these signals must be processed before they lead to very "cells". When we say topology, we mean the fact that the TDI takes a serial input of BSR, taken as a TDO serial output. On the other hand, however, the TCK(Clock) and TMS are conducted in parallel to each BSC.

When we say functional, we mean the fact that on the basis of signals generated by other (Update-DR, for example). For this reason, the TAP complex is accompanied by a digital circuit whose name according to the standard, followed by TAP kontroler. Thus, the TAP controller is a sequential machine with 16 states that, in fact, acts as a protocol for the implementation of testing.

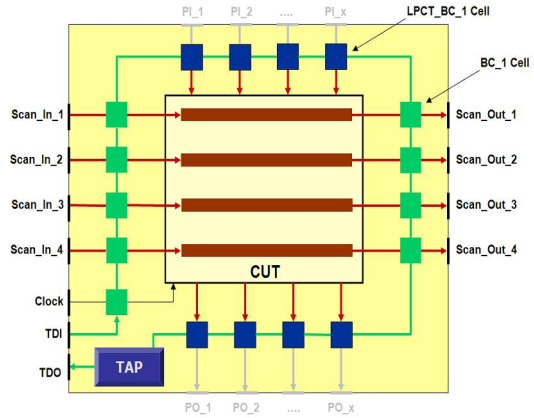

Fig.4. *Boundary Scan Access to Functional I/O Pins*

For example, consider this, compared BS concept and consideration in this paper, Fig. 4 depicts the basic configuration for this approach which eliminates the need for the tester to connect to the primary input and output pins directly.

In order to enable the use of the TAP controller and facilitate functional pin access through the Boundary Scan Register (BSR), certain modifications are necessary in the BSR. In this test mode, the TAP controller is placed in the Shift-DR (Data Register) state, and the control signals for the boundary scan cells are bypassed. As a result, the signals for shifting and updating data on the boundary scan registers are generated by the tester. In this manner, the boundary scan cells can be fully controlled, regardless of the controller's state.

This greatly simplifies manufacture testing by using boundary scan cells since they will act as standard scan cells without continuously manipulating the TAP state machine.

3.6 5-pin TAP Only Tessent TestKompress

This low pin count test strategy utilizes the 4 or 5-pin TAP interface to control all scan hardware as well as the functional I/O pins using the techniques described in the previous section.

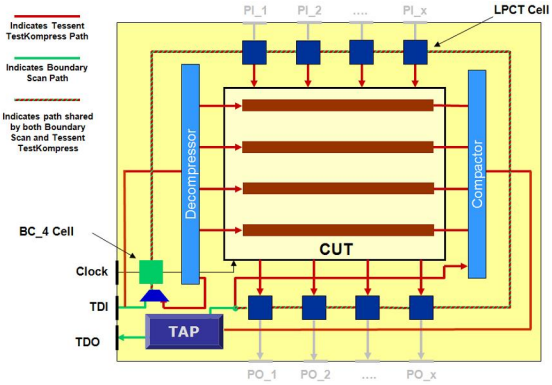

Fig.5. *Design using only TAP port to control Tessent TestKompress and boundary scan logic*

The ability to test the design deterministically using only the TAP ports makes it possible to test CUT or DUT that the design on board and in system as well as on the ATE.

Fig. 5 shows a high-level view of how a single Tessent TestKompress scan channel and boundary scan register are controlled through the TAP ports.

The test patterns which are normally applied to the primary I/O of the device can now be compressed as part of the scan patterns stored on the tester.

In this configuration, Tessent TestKompress provides a dramatic compression of the test data and the application time, while the TAP interface eliminates the need for functional I/O access. Using this technique on sub-block and/or core applications, large amounts of test data can be delivered to the core in a small amounts of time and with few connections to chip-level pins.

3.7 3-pin Only Tessent TestKompress

Test pattern generation typically requires the test structures and the test control pins which are controlled during the test. Typically, these test control pins such as scan enabler, scan clock and resets are available at the top level for ATPG to control. When running the Tessent TestKompress, two additional test control pins are required (edt_update and edt_clock). In some situations, however, there are fewer than required top level pins that exist for the test purposes. In order to run ATPG, these control signals need to be driven by some internal logic block to ensure that the generated patterns are valid and accurate.

The basis of ideas that allows the implementation of these requirements is to add cell shift register with each input/output interface components.

BSC are memory elements that are distributed across the edge of the integrated circuit. Primary input signal must pass through a BSC to arrive a system of logic. Also, the signal from the output of the system logic must pass through a BSC to reach the primary outputs, as shown in Figure 6.

BS cell has two data inputs, four control inputs and two outputs. At the same input Scan In-TDI and Out-scan output TDO are serial, and when excluding the first and last BS cells, information are transported through the BSR. Other inputs and outputs are parallel. This means, for example, that the control signals CLK A, Test mode select, Shift / Load and CLK B common for all BS cells.

The requirements for using only 3 digital pins (scan in, scan out, clock) with the Tessent Test Kompress are to maintain high compression, provide an X tolerant solution, maintain the same high stuck-at and transition fault coverage, and maintain diagnosis capability of compressed patterns. The appearance of a BSC is shown in Fig. 6.

All of these requirements can be met using a test controller that generates all necessary signals internally.

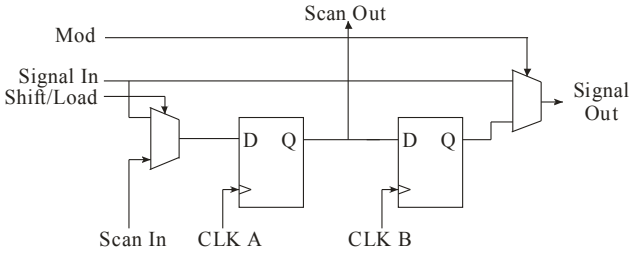

Fig.6. *Boundary scan cell*

The original hardware implementation for the 3-pin test controller was done as a custom block, which addressed the stated requirements while reducing test application time and test data volume by 25x.

The test controller implementation flow is now being fully automated in the Tessent TestKompress and will be generated as a part of the standard logic when specified by the user.

4. CONCLUSION

Research results shown are related to the problem of testing and diagnosis of digital electronic circuits. Problems related to short transition times were discussed first. Then impact on testing technology was considered including the ATE performance for different types of circuits under test.

Accordingly, new design architectures were discussed enabling design for testability with low pin count testing is an effective solution for reducing structural costs in the IC manufacturing environment. By combining LPCT with test compression, extend the capabilities of manufacturing testing to allow application of at-speed test patterns using low-cost testers which are very pin-limited. Using the Tessent TestKompress with LPCT enables improvements in test coverage and application time with minimal impact on design and test overhead.

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