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A VLSI TESTER FOR IC TESTING AUTOMATION

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Abstract – ***The performances of a tester are investigated so getting a base for further research and development of an inhouse testing laboratory equipment.***

1. INTRODUCTION

Testing of integrated circuits (ICs) is of essential importance for their design [1], production and application [2]. In the design phase it is necessary to develop such a method which will enable systematic testing in the successive phases. In the phase of production (manufacturing) correctness of the circuits is established. In this context, testing is possible on the pellet, before encapsulation, but testing is necessary after encapsulation, too. Taking in consideration that huge series are in question, testing of produced chips in semiconductor industry is of essential importance from the economy of production point of view. That means that testing devices, the so called VLSI testers, have, in addition, to fulfil one very important requirement: very high productivity. Finally, in the exploitation of the component phase, the importance of testing is twofold. First, for verification of acquired (purchased) components, and second, for verification of components from the company store.

Taking all this into account, and having in mind that the performance of the tester must always exceed the performance of the Device Under Test (DUT), one may conclude that the VLSI tester is a very expensive device. Prices of such devices are up to several million $. Design of VLSI testers are, as we can see, very hard task. Nevertheless, for some low productive uses, such as laboratory-verification of small series, it's not necessary to obtain all the highest demand performances, so a need arise for design of specific testers which will be developed under lower price. In this research, the way of taster work will be described [3], together with it's characteristics and it's application.

The tester will be viewed as a highly automated device containing three main components: the computer system used for "testing programming", the electronic subsystem enabling the synchronisation, waveform generation, and DC signals supply, and finally, the measuring head enabling contact with the DUT. High productivity, especially in the semiconductor factory environment, means excellent mechanical and electronic co-ordination, co-ordinates and pattern recognition etc. All this properties will be taken into account when considering design requirements for a VLSI tester.

2. CONCEPTS IMPLEMENTED FOR TESTER DEVELOPMENT

There are three main components of the VLSI tester system. First of all, there is computer system which is used for testing programming. Then, there is electronics subsystem which provides synchronization (timing), waveform and DC-signal subsystem, and at last there is testhead and pin electronics which provide direct contact with the tested component. It's known as DUT-device under test. The architecture of the VLSI tester is shown on Fig. 1. Some basic characteristic of subsystems will be consider in following text.

A. Control computer subsystem

The computer subsystem, represented on Fig. 1, (shown as "Computer control of the testing"), performs wide spectre of activities, which are constituting the testing such as: mode of work, generating testing sequences, programming of signal distribution, and reception and storage results of measurement, diagnosis etc. Description of components (pin numbers, position of functional pins, together with description of functions and defects) which are tested are entered on a specific language dedicated to description of testing which is determined by producer. Sometimes, when known test signals are given, during the test description of input signals, one may enter the input stimuli interactively in a form of column of binary words. Instead, for complex circuits, especially for circuits produced outside of the testing site, it's recommended to perform synthesis of test during component's design phase. Of course, for laboratory conditions, when intensive testing is not necessary but the sequence is checked only, it is possible to use the tester for synthesis of test message too.

The tester work under control of this unit goes in following way. After starting, configuration data are placed on bus. They speak about correspondence between "program pins" and real physical pins on chip. Then, under the control of the clock, test words are brought on bus one after another. The end of the entering massage are recognized by some characteristics world (for example, all 1111..). For pins that are configured as input pins , signals come from bus on chip via threestate buffers. On the other side, outgoing pins produce signals that are led immediately to a comparator and compare with "correct" signals that exists on bus. If disagreements doesn't exist , the next command are executed since the test is not finished. If disagreements happened error signal are sent to the controller and it stops the system and produces error state as a result of testing.

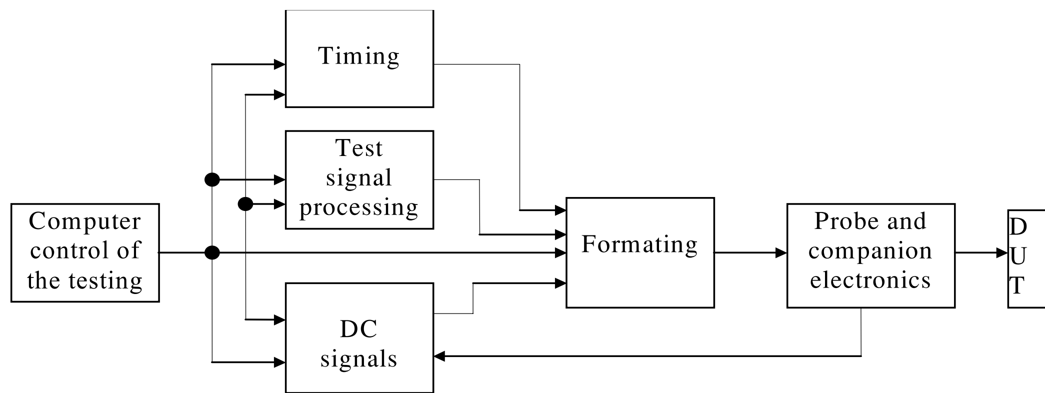

Figure 1. *Architecture of a electronic tester*

The computer system used may be organized hierarchically. This mins that there are design stations communicating the testing system. In such a configuration a second level of computer control is contained at each test station, thus allowing it to operate independently of the system controller once it has been loaded with appropriate test programs.

Since different circuit technologies dictate different signal and impedance levels , the pin-electronics section at each test station provides high voltage for TTL and MOS unipolar chips and low voltage for ECL bipolar parts. Instead of mechanical relays, electronic switching is used to provide faster and more reliable testing.

Test station may be programmed in several languages, allowing users to select a familiar language or one most suitable for a specific test application. A common interface allows a routine written in one language to be called from a program written in another. Languages supported include the Abbreviated Test Language for All System (Atlas), Pascal, FORTRAN, and Comprehensive Tester Application Software (CTAS). The latter language enables inexperienced in any of the supported languages, to rearrange the order of sequences, and to modify test specifications where necessary.

Once a complete VLSI test vector set has come onto existence , we must then verify that it does everything that it is supposed to do: exercise and test the chip in a way that is both accurate and complete. With test software that has been generated manually, every step (test vector) in the sequence is comprehensible and checked by the test engineer for errors that have been generated manually.

By contrast, the complexity of VLSI test programs and CAD/CAT-generated test vectors makes it unrealistic to check each step in the test sequence manually. Fault-simulation and logic-modelling errors could show up in the automatically generated truth table. The test program must therefore be checked or verified.

One way of verifying the integrity of software that has been generated by fault simulation and logic modelling is to run such programs against a discrete implementation of the VLSI chip. First, the test vectors are fed as inputs to the discrete implementation, and then the outputs are monitored for functionality.

Another method is to use software simulation to exercise the input, output, and associated routines under conditions approximating those of actual test operations, without using the tester itself. The problem here is that errors contained in the CAD/tester process for logic modelling and fault simulation are further simulated – and thus they are also compounded.

B. Timing subsystem

One of the most important aspect of the tester's work is the synchronization. Duration of signal's edge are measured by hundred pico-seconds (or less) and discrepancies exception (deviation) in this domain will probably be treated as wrong logic conditions.

The term timing will be used not only to express synchronization, but express control of logic conditions too, for the tester should not always work with the fastest clock.

A typical shared-resource architecture includes a master clock generator, a number of timing generators (generally fewer than 20) followed by a complex switching matrix to distribute timing signals to waveform formatters, and a pin-electronics drivers and comparators. Since a large number of different paths are possible through the switching matrix for ICs with high pin counts , signal delay (or skew) varies for different input/output pin combinations, making calibration or deskewing difficult. Another serious obstacle with shared resources is the lengthy programming time that is required to schedule the routing of timing signals through the switching matrix.

A straightforward arrangement is to provide every pin of the chip to be tested with its own testing resources, or test-per-pin architecture. Thus each pin is supplied with a programmable high-speed timing generator, waveform formatter, DC parametric unit, pin driver, pin comparator, and programmable current load. Since there is no longer a need to switch signal routing, greater accuracy is possible. Also, software is simpler and faster to develop, and the tester–per-pin modular structure permits higher pin-count sections to be added conveniently. Shared-resource architecture is less costly, obviously, since less hardware is demanded, but the tester–per-pin approach seems to become

more appealing as the complexity of the chips being tested increases.

On–chip testing has surfaced as a viable way of testing VLSI ICs more effectively and will have to be taken into account by new generations of test gear. Called by various names, including scan-path, serial-scan, and level-sensitive-scan-design (LSSD), the technique structures the logic so that its response is independent both of the order in which inputs change and circuit delays between logic elements. Thus the IC is converted from a time-dependent sequential circuit to a combinational circuit. The key advantage is that combinational circuits are responsive to truth-table analysis, while sequential circuits are not, and truth tables can be generated quickly and efficiently by large computers. Although roughly 20% more silicon is required on the chip for the added test circuits, design can be checked using the serial-scan technique.

Talking about characterization of signals on output pins of the DUT, two types of measurements are usually possible. There is a possibility of work in so-called window mode. That means that time interval is given and one checks whether the expecting signal change happened on output pin. Second work mode is comparison of pulse edges. In this case types of expecting edge are supplied.

C. Test signal processing and format subsystem

In this subsystem generation of electrical signals are performed under the computer control. For every input pin impulse column are formed with exact distribution of zero's and unities. Pulse amplitude (in volts) which is generated must be programmable too. Forming of signals means in fact determination of possible state of system work for every pin. For input pins one should have a set of commands such as: Input Formats: Off(3-state), Return to One, Return to Zero, Return to Complement, Non-Return, Surround by One; Output Formats may be: Expect One, Expect Zero, Expect 3-State, Don't care ("Mask"). This subsystem may also perform some specific functions that enable effective work of the tester with lower complexity of the electronic circuits which would be used later on. For bringing the signal on two neighbouring pins multiplexing signal electronics could be used. On the Fig. 2. example of this effect is shown.

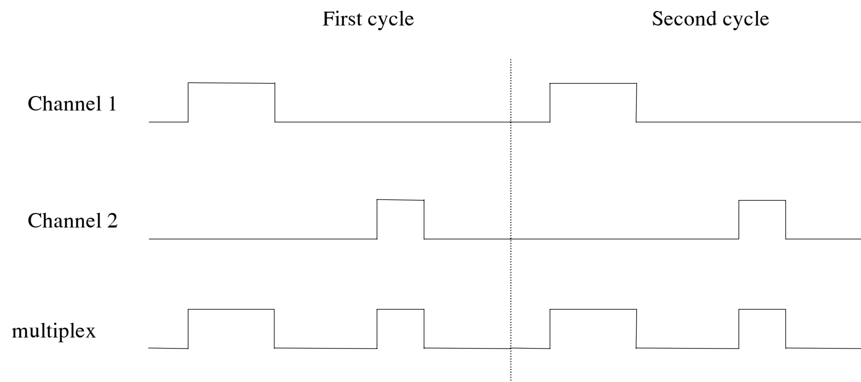

Figure 2. *Multiplexed signals to avoid interference*

D. DC subsystem

As Fig. 1 shows the DC subsystem has multilateral communications with its environment. First of all, this subsystem delivers power to DUT. Some components such as ones produced in BiCMOS technology may demand more sources with different voltages for power supply at the same time. It's necessary to supply a wide range of stable voltages with very low output resistances delivering considerable power (which, of course, becomes higher during the work on higher frequencies). From high productivity point of view, quick establishment and decay of power supply voltage, may be of importance.

For the other hand, DC subsystem is that which in accordance with power supply control, determines the amplitude of the impulses used for functional testing too, as it was said before.

Finally, the power supply subsystem is measuring the supply current, the so called I_{ddq}, which in some testing techniques has a decisive role. I_{ddq} is used often in diagnostical purpose too.

Example current values, for one tester [4], are the following. For the input pin the current spans over the interval from 238 nA to 62,5 mA, while the supply current may reach even 1 A. Signal voltages span between -4 V and +16V.

E. Probe and appropriate electronics

The tester of universal uses (not specialized for pellets for example) has a probe in the shape of moving "hand", which is installed on various stands. Quantity of electronic in probe itself is minimized and contents only one threestate buffer per pin, usually. In this way, signals are obtained to reach frequencies up to 800 MHz on pins. The main port of electronics are placed in tester itself and are connected with the probe with coaxial cable of high quality. To obtain such fast work of tester, the dissipation in electronic is large, so the great, heat are generated. That's why the tester demands intensive cooling. For some devices cooling is done by air, but very fast and high productive systems use liquid nitrogen.

Taking in charge that some tester users are specialized in manufacturing semiconductors components, as for example ASIC circuit, memories, PLAs and similar, producers of testers offer various probes and electrical environment for given design stiles. In that way, users are free from

unnecessary complexity of testers and in such way greater productivity in the phase of testing is enabled.

VLSI test system that can simultaneously test one, two or three test heads (probe) are definitely cost effective. Within each test head, it is important to have multiple high speed DC voltage and current measuring circuits since DC measurements can restrict the testing through-put of large pin count IC's. Costs can also be reduced by software that makes a VLSI test system easy to program.

F. Common demands

In this paragraph some technical characteristics that describe the VLSI tester as industrial device will be mentioned. Among them, important are physical dimensions, electronic characteristics, possibility of superstructure and similar.

For [4] example, the following characteristics are valid:
a) View of dimension
Basic device: 100 In x 50 In x 80 Inch (length, width, height), weight 1350 kgr;
Two power supply are used 208 V,100 A;
In condition of clean room, it demands 16 t of air for a day for air-conditioning.
Price: $1,3 million for common; this price represents excellent compromise of price and performances.
b) Characteristics:
Testers are used for integrated circuit testing with up to 512 pin;
Maximal speed of testing is 100/200 MHz;
In central memory up to 8 MB test vector could be memorised;
c) Possibility of further superstructure of tester
Ability of testing integrated circuits up to 1024 pin.
Improvement from the view of testing speed up to 400 MHz
Upgrade of possibility of testing integrated circuits that are designed for testability (Boundary Scan as IEEE 1149.1 standard for example [5]
d) Reconfigurability
Resources for testing are divided in levels up to 128 pin;
There is possibility of upgrade with additional levels 128 pinone level; 256 pin two levels; 512 pin- four levels. That enables best use of the tester's resources.

3. CONCLUSION

Testing of integrated circuits is activity of great importance in all phases of one components life. That's why systems for testing are of essential importance for verification component and by that for supply electronic devices quality in which they are built. Talking in terms of complexity of components and greater speed of work, very complex demands are placed in front of testers. The same may be said for the managing (software supply) and for the technological realization point of view. So, it could be said that testers demand the finest and the most expensive electronics. Their prices has never been low, independently of electronics components price fall. The reason for this is the higher and higher level of performances of this devices.

In order to meet these challenges IC's designed for laser repair, easier testability, or self-test, will become mandatory. Contact-free laser techniques may become the dominant measurement method for characterizing GaAs IC's operating at rates above 1 GHz.

In this work (paper) the very first effort were made to recognise VLSI testers characteristics and all for the purpose of creating conditions for development of laboratory equipment. It's expected that knowledge generated during this research will enabled more efficient and rational uses of this expensive and sophisticated systems at our laboratory.

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